A Control System for Atomic Fountain Clock Based on Field- Programmable Gate Array

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***Abstract*— A control hardware for atomic fountain clock based on a field programmable gate array(FPGA) is presented, which can output 20 digital transistor-to-transistor logic(TTL) signals with resolution of 40 ns, 10 arbitrary waveforms and acquire 8 analog signals. Both outputs share same reference clock and trigger signal which ensures that all output signals are output in a synchronized well controlled way with a maximum timing error 500 ns. Moreover, The data acquisition and clock servo function is also integrated on FPGA. FPGA communicates with a PC by Ethernet. All the data are saved at the PC.**

Keywords—atomic fountain clock; FPGA; control hardware; arbitrary waveforms; clock servo;

I. INTRODUCTION

Atomic fountain clock operates in sequence mode. One cycle consists of atom collecting, launching, post-colling, state selecting, interrogating and detecting. Then the TOF(time of flight) signals are acquired and the frequency of the Hydrogen clock is locked to the atomic resonance of the atomic resonance of the fountain clock. every step requires precise timing control dozens of the experiments such as the intensity and frequency of the laser. In addition to output timing signals, the data acquisition system (DAQ) and clock servo functions are also integrated to the Control system. The procedure is achieved by four output types: digital TTL outputs are used to control the magnetic field shutter, microwave shutter, laser switch and so on. DAC(digital to analog converter) outputs are required to generate arbitrary waveforms in order to control the laser intensity. ADC(analog to digital converter) is used to acquire TOF signal at specified time every cycle. Peripheral output such as Rs232 is used to control the frequency of DDS(direct digital synthesis) for realize servo function. Control system used in Cesium fountain clock before is based on NI(National Instrument) hardware and software[1]. No matter the hardware is based on PCI or PXI platform, it needs multi boards and responding terminal blocks, cables[2], which take up more space. Moreover, These multi boards are required synchronized by configuring in software. While FPGA-based control system is compact and flexible, which is already applied in many atomic, molecular and optical experiments [3-11]. Here we present a control system based FPGA. Three output types are integrated on one printed circuit Board(PCB) which simply the synchronization method. All signals are output in a well synchronized way. Additionally, the timing and servo part can be operated independently.

II. SYSTEM ARCHITECTURE

The hardware is composed of 5 parts. FPGA ADC DAC 、power supply circuit and peripherals. The block diagram of a typical setup of a control hardware is shown in Fig. 1. The main module is FPGA consisting two parts: the processing system (PS) and the programmable logic (PL). To communicate between the FPGA module and the ADC, DAC modules, the Serial Peripheral Interface (SPI) protocol is used. FPGA module communicates with a computer via Local area network(LAN). The chip XC7Z020-2CLG484I from Xilinx FPGA module is adopted to output digital TTL signals. The output logic level of the I/O on the FPGA is 3.3 V. The level translator SN74LVC4245APW is applied to translates 3.3 V to 5 V logic level. Three DAC chips AD5754R with 16 bit resolution and 4 channels are chosen to generating analog waveforms. One ADC chip LTC2335-16 with sampling frequency of 1 MHz and resolution of 16 bits is adopted. All the modules operate sample clock signals at internal FPGA 50 MHz signal or an externally referenced 10 MHz clock through SMA connector. And all outputs share the same trigger signal which is provided from the first TTL signal or external TTL signal. Power for FPGA is supplied by DC/DC chip. Power supply for analog circuit is fed by DC/DC and low-drop-out (LDO) chips. Peripheral modules consist of one Rs232 interface and two Ethernet interfaces. The level translator MAX3222EEUP is adopted to translates LVTTL to Rs232 signal. One Ethernet interface employ the physical layer(Phy) chip 88E1116R which is linked to Ethernet controller embedded in the FPGA to control commercial instruments. The other network port is extended by microcontroller(MCU) which

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is connected to the FPGA through the flexible static memory controller(FSMC) bus. The printed circuit-board(PCB) is a 8-layer board design. The whole control system is installed in a box. All the connectors on the front panel are SMA interfaces. Ethernet network and power connectors are located on the rear panel. The whole board is pictured in Fig. 2.

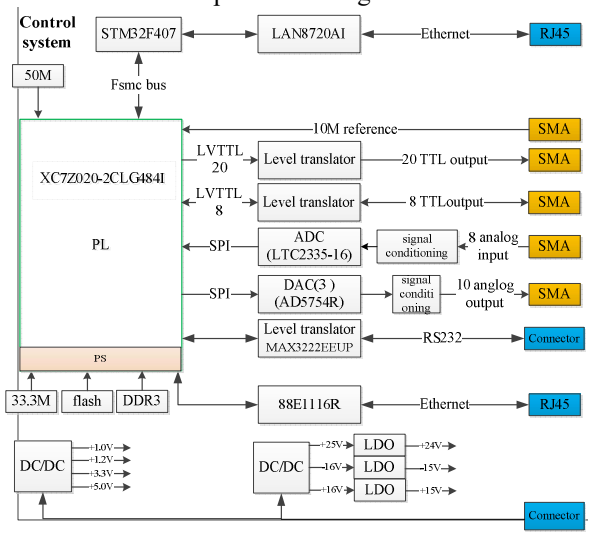

Fig. 1 Schematics of the control hardware

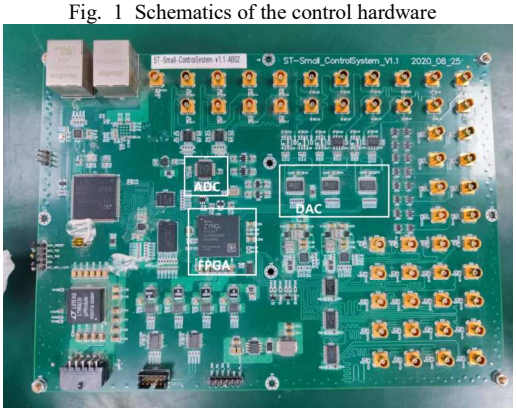

Fig. 2 The picture of control board

A. FPGA module

The host computer sending the LVTTL time parameters to the PS side through the network port protocol, and PS side send these parameters to the FPGA side through the AXI_lite bus internally, then the FPGA start to generate pulses. After the FPGA collects the pulse time information from the PS side, it starts to wait for the trigger pulse to trigger the time counter. The pulse signal judges whether the counter is in the period of the reversion pulse, so that the LVTTL waveform is reversed, otherwise, the original waveform is maintained. The time counter will continuously counting cyclically according to the cycle set by the host computer, so that the LVTTL waveform can be generated cyclically. Two TTL pulses can be generated in one cycle. Every TTL outputs can be set to constant 5 V or 0 V in order to test in the experiment. Light emitting diodes(LED) illustrates the output status of the TTL signals. When TTL output is in the high level, LED is green, else LED is off.

B. DAC modules

When the AD5754R is powered on, the power-on reset circuit ensures that all registers are defaulted to 0. then all channels and the internal reference voltage source is shutdown. Otherwise, the first write operation to the device may be ignored. When first communication with AD5754R, the voltage write for all channels should be set to the required output range by writing to the output range selection register (the default range is 5 V unipolar range). Then, we should write to the power control register to power the desired channel and internal reference voltage source (if required). If an external reference voltage source is used, the internal reference voltage source must be shutdown. The specified waveforms are output according to cycle time and sweep time which don't need to load to the memory. The parameters of analog output waveforms are calculated by PS according to the logic requirements and send them to the FPGA. The counter in the FPGA judges the changing time of waveform and writes to the DA frequency control word cyclically. Then the FPGA refresh the waveform in real time. Performance result of DAC can be seen in Fig. 3. There is a 1.0 µs settling time for a 5 V voltage change shown in the inset. Delay between two DAC chips(DAC1 and DAC2) is 2.6 µs.

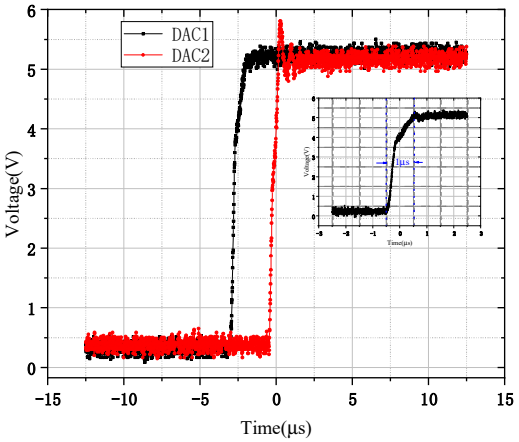

Fig. 3 Performance of DAC boards. The inset shows settling time for a 5 V voltage change.

C. ADC module

ADC chip has 8 acquisition channels. When write to channel cyclically from channel 1to channel 8, we can get the voltage value collected by channel 1~8, the voltage value is displayed in 16 bit binary format, and the collected data of channel 1~8 are respectively stored in 8 FIFOs which are allocated by FPGA memory to complete the data buffer. The ARM side regularly reads and writes the data in the FIFO, processes the data and uploads it to the computer. Then the upper software completes servo feedback algorithm, and finally obtains the calculation value.

The acquisition is retriggered at every cycle. The PS on the FPGA judges the reading mark sent by the FPGA. After the mark is received, the data in the buffer FIFO of the current period is completely read. FPGA side will wait for the parameters including acquisition time send from the upper computer after it is powered on and reset. when the trigger pulse arrives, FPGA starts to control the ADC chip to acquire the signal, and store the data collected from channel 1 to channel 8

respectively to the corresponding buffer FIFO, then the FPGA send the reading flag to the ARM, and waiting for the ARM to empty the data in the buffer FIFO. Then the next cycle repeats the above work.

D. Power supply

The power supply circuit is mainly composed of FPGA power and analog circuit power. The power for FPGA is supplied by DC/DC TPS65261RHB which can convert 12 V power to three outputs, respectively 1.0V, 1.2V and 3.3V. In order to reduce power supply noise, the analog part uses low-drop-out (LDO) power supply. First, the 12V power supply is increased into 25 V and 16 V through the DC/DC chip ADP5070, and the 25 V and 16 V are converted into 24V and 15V power through the LDO chip.

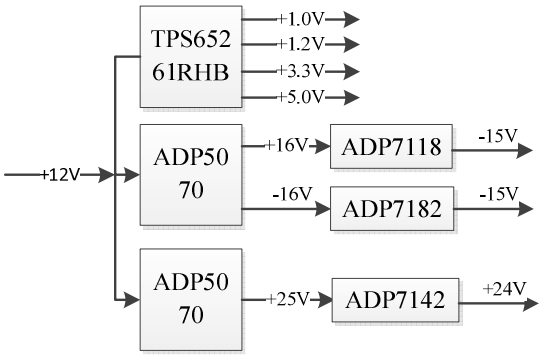

Fig. 3 Block diagram of the power supply

E. Software

Control software running in PC provide graphical interface to communicate with FPGA. IP addresses of FPGA is fixed. Firstly, software connect to the TCP/IP port on the FPGA and send parameters to FPGA. All the parameters consist of control parameters, timing parameters, analog output parameters and acquiring parameters can be configured on the interface displayed as Tab page. control parameters compose of cycle time, nominal frequency and PID parameters. Cycle parameter can be set from 1ms to 3 s. Timing parameters including trigger level, delay time, during time in high level of each TTL. Time in low level is calculated by software according to the other parameters. analog output parameters including initial voltage, scanning time and stop voltage. TOF signals are acquired and displayed on the interface. The software calculates the frequency stability in real time according to difference between the frequency of the atomic transition and synthesizer. And data such as atom numbers, transition probability are saved to a file. when the software is once started, it will be run repeat indefinitely until user stop it.

III. DISCUSSION

The control system is operated all functions of the timing, data acquisition and servo frequency lock of the atomic fountain clock successfully. There is no need to create the large output buffer for the analog and TTL outputs. Synchronization between multi-channel outputs is critical for fountain clock. The amplitude of the TOF signal will get lower over time. Figure 4 is synchronization result between one of TTL and analog output. The two signals are output at the same time. The delay is between these two signals is 500 ns. This control system is applied in cesium atomic fountain clock at NTSC. The frequency instability is same with the result using NI control system which is shown in Fig. 5.

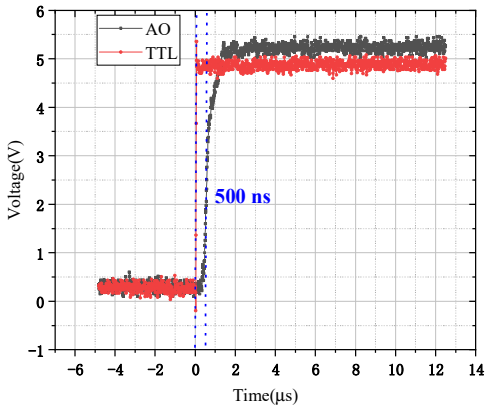

Fig. 4 delay between one of the AO output and TTL output during a sequence

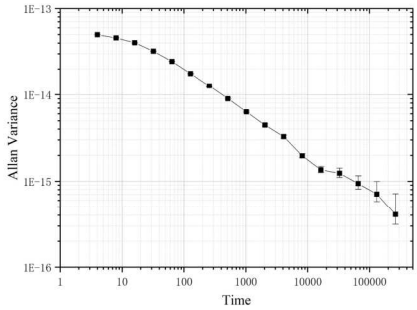

Fig. 5 Allan deviation of NTSC fountain clock for high atomic density

IV. CONCLUSIONS

The control system based FPGA is designed and realized for atomic fountain clock. it is compact and don't need extra configure synchronization between multi boards. It is already applied in Cs fountain clock and has been shown to be a robust system. It can also extended to other atomic clock.

ACKNOWLEDGMENT

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